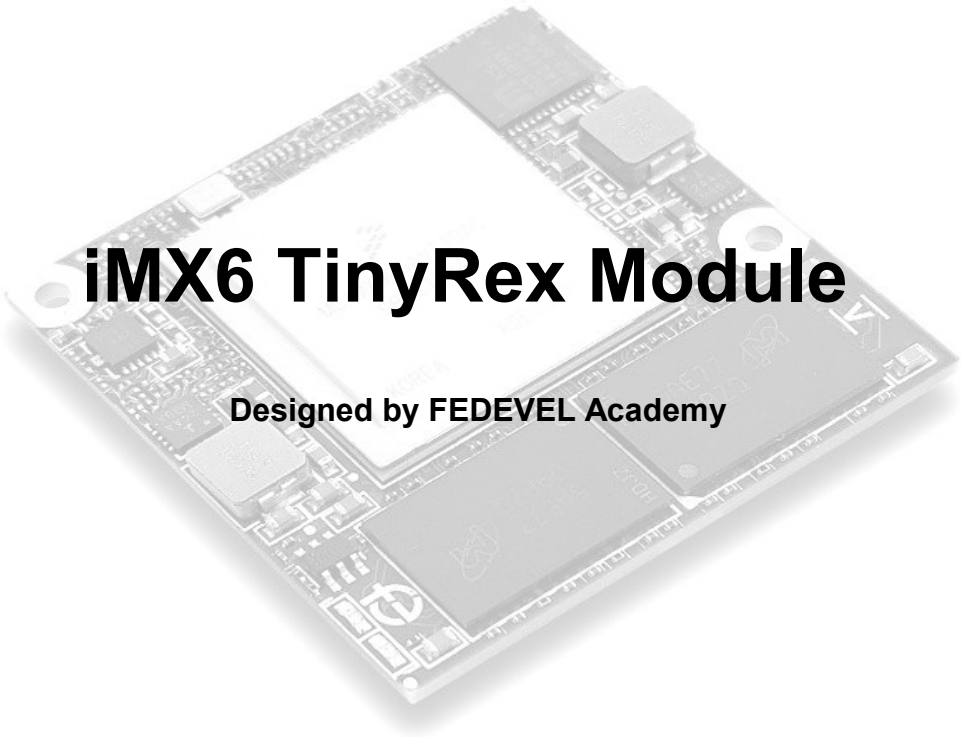
voipac



iMX6 TinyRex Module

Designed by FEDEVEL Academy

Datasheet

Date	Revision	Changes
February 12, 2016	1.0	Initial Release

Table of Contents

1. Introduction

1.1. Hardware

The iMX6 TinyRex Module represents the next generation of advanced multimedia, power-efficient and cost-effective solution for embedded systems, and was designed by FEDEVEL Academy, which focuses at ARM boards Schematic and PCB design courses. With preinstalled operating system and running up to 1.2GHz, the module enables designing of high-end products with quick set-up and easy-to-handle programming of own applications.

The scalable and compact iMX6 TinyRex Module is the second member of growing family of REX boards. Equipped with single or multicore i.MX6 ARM Cortex A9™ CPU, it supports features such as integrated display controller, full HD capability, enhanced graphics and connectivity. Compared to its predecessor, iMX6 TinyRex Module is half in size but provides access to almoust all of the i.MX6 CPU pins available, including the camera interfaces. It also offers unique HDMI input interface, and is tuned for large volume applications.

The core component is the high-performance NXP / Freescale i.MX6 advanced multimedia processor with very low power consumption. Only 1.60 mm thick 12-layer HDI micro-via PCB of the module further carries up to 4GB DDR3 SDRAM, Gigabit Ethernet, I2C EEPROM, and other chips thus providing vast majority of the embedded systems must-have peripherals.

The iMX6 TinyRex Module is highly scalable and available in 4 standard hardware configurations: **LITE** / **BASIC** / **PRO**fessional / **MAX**imum, each equipped with three 100pins board-to-board connectors. Manufacturing of customized configuration of the module is available upon request, minimum batch size is 10pcs. A standard configuration COM is manufactured in 0°C to +70°C commercial temperature range. Upon request, the module is available also in -20°C to +70°C extended operating temperature range, or in -40°C to +85°C industrial temperature range.

VOIPAC provides free access to available documentation, and each complete development kit comes with the iMX6 TinyRex Computer on Module schematic and Altium Project files of the iMX6 TinyRex Base Board Lite stored on a USB stick.

1.2. Software

Voipac fully supports Linux operating system with drivers for all basic interfaces. Custom additional drivers for specific applications can be developed upon request.

Operating system	Description
Linux	Yocto Project (Filesystem installed on microSD Card)

1.3. Booting Options

The standard configuration iMX6 TinyRex Module comes with e-Fuses set for direct boot from microSD card located on the iMX6 TinyRex Base Board Lite. There are more booting posibilities:

Booting Option	Description
SD Card	A standard configuration module e-Fuses are set for this boot option
I2C	EEPROM mounted on the module (I2C1 Only)
SPI	Only with SPI Flash on TinyRex Base Board Lite (SPI1 Only)
SATA	Only with i.MX6 Quad and i.MX6 Dual processors
Other SD Cards	
NAND	

The module supports all booting options:

- Boot From e-Fuses: Standard mode
- Serial Downloader : USB mode
- Internal Boot: Depending on values of GPIO pins, boting device is selected (without the need of changing e-Fuses settings) - Not supported by TinyRex Base Board Lite

1.4. Features Summary

Feature	Description
CPU	i.MX6 ARM Cortex-A9™ CPU (NXP / Freescale), clocked up to 1.2 GHz / up to 4 cores
DDR3 SDRAM	DDR3-1066 SDRAM (533MHz), up to 4GB
I2C EEPROM	Up to 512kBit
NAND FLASH	1x NAND Flash or 1x MMC (8bit)
SD Card	2x SD (2x 4bit or optional 4 & 8bit)
VIDEO	• HDMI (up to QXGA 2048 x 1536) • LVDS (up to WUXGA 1920 x 1200) • 20-bit parallel LCD display (up to WXGA 1366 x 768) or 20-bit parallel Video Input (CSI) • 20-bit parallel video input CSI (up to 8192 x 4096) • DSI MIPI differential display output (up to XVGA 1024 x 768) • MIPI differental camera input
AUDIO	Digital Audio
ETHERNET	10/100/1000 Mbps
USB	2x High-Speed USB 2.0 OTG/HOST
OTHER IO	5x UART / 2x GPIO / 2x GPIO or PWM / 3x I2C / 2x SPI / 1x CAN
OTHER HIGH SPEED	1x PCIE, 1x SATA
SYSTEM SIGNALS	RESET IN/OUT, BOOT MODE, POWER OK, USER BUTTON

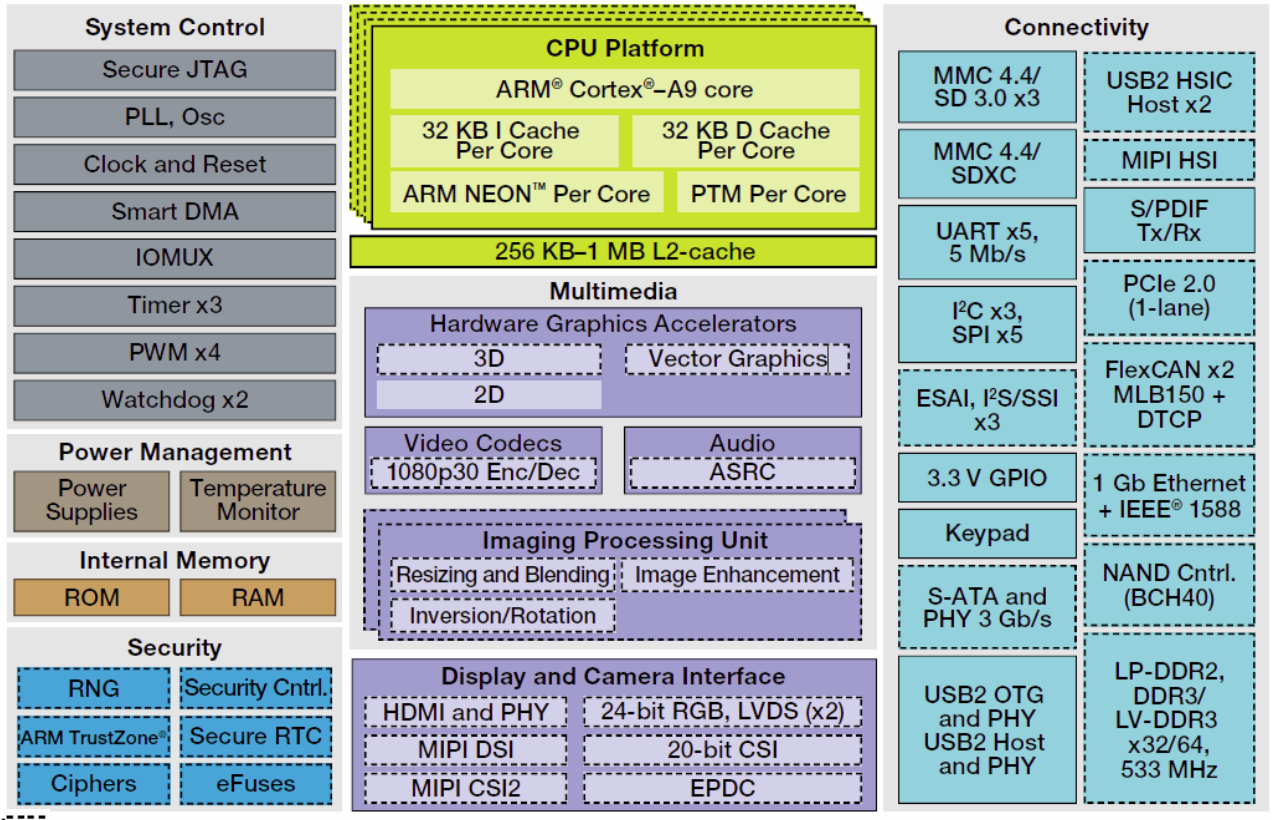
1.5. Reference Documents

For more detailed technical information about the iMX6 TinyRex Module components, please refer to the web resources and documents listed below.

Component	Manufacturer	Description
i.MX6 Processor	NXP / Freescale	i.MX6 Quad / i.MX6 Dual / i.MX6 Solo
DDR3 SDRAM Memory	Micron Technology	MT41K256M16HA-125:E, MT41K128M16JT-125, MT41J64M16JT-15E
I2C EEPROM	ATMEL	AT24C512C-MAHM-T, AT24C256C-MAHL-T, AT24C128C-MAHM-T
Ethernet Controller	Microchip Technology	KSZ9031RNX
PMIC – Voltage Regulator	Texas Instrumets	TPS74801DRCR
PMIC – Voltage Regulator	Intersil	ISL8024AIRTAJZ-T7A
PMIC – Voltage Regulator	Micrel, Inc.	MIC33050-4YHL TR
PMIC - Supervisor	Texas Instrumets	TPS3808G09DBVR
Logic-Gates and Inverters	Texas Instrumets	SN74AHC1G09DCKR

2. Functional Processor Description

2.1. *i.MX 6 Series Applications Processors Block Diagram*



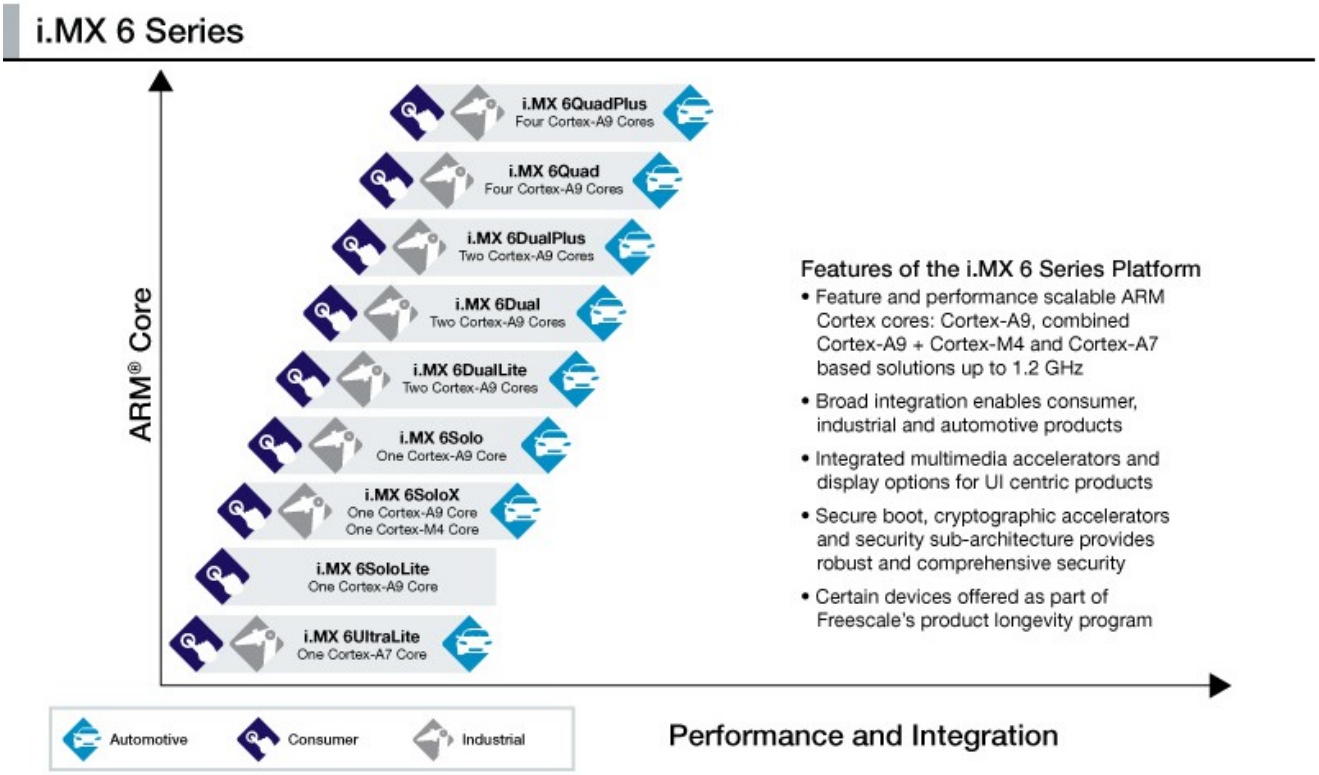
Available on certain product families. More information in interactive table on NXP/Freescale's webpage

The i.MX6 processor features NXP / Freescale advanced and power-efficient implementation of the ARM® Cortex® A9 core, which operates at speeds as high as 1,2 GHz. Up to 533 MHz DDR3 and mobile DDR DRAM clock rates are supported. The CPU is suitable for the following applications:

• **Tablets**	• **Smartbooks**	• **E-Readers**
• **Home audio systems**	• **Home energy management systems**	• **Portable medical devices**
• **Automotive infotainment**	• **In-flight entertainment**	• **Point-of-sale devices**
• **Digital signage**	• **Intelligent industrial control systems**	• **Vehicle to vehicle connectivity**
• **Human-machine interface**	• **IP phones, IPTV**	• **Secure smart-connected devices**

More information in interactive table on NXP /Freescale webpage

2.2. Features



i.MX6 Quad
Quad ARM® Cortex®-A9 up to 1.2 GHz
• 1 MB L2 cache, NEON, VFPvd16 TrustZone • 3D graphics with four shaders • Two 2D graphics engines • 64-bit DDR3 and 2-channel 32-bit LPDDR2 at 533 MHz • Gigabit Ethernet MAC • Integrated SATA-II • HDMIv1.4 controller plus PHY • LVDS controller plus PHY • PCIe controller plus PHY • MLB and FlexCAN controllers

i.MX6 QuadPlus (Module is designed to support this processor)
Quad ARM® Cortex®-A9 up to 1.2 GHz
• 1 MB L2 cache, NEON, VFPvd16 TrustZone • **Enhanced** 3D graphics with four shaders • **Enhanced** Two 2D graphics engines • **Prefetch & Resolve Engine** • **Optimized** 64-bit DDR3 and 2-channel 32-bit LPDDR2 at 533 MHz • Gigabit Ethernet MAC • Integrated SATA-II • HDMIv1.4 controller plus PHY • LVDS controller plus PHY • PCIe controller plus PHY • MLB and FlexCAN controllers

↓↑ **Red indicates change from table to the left**

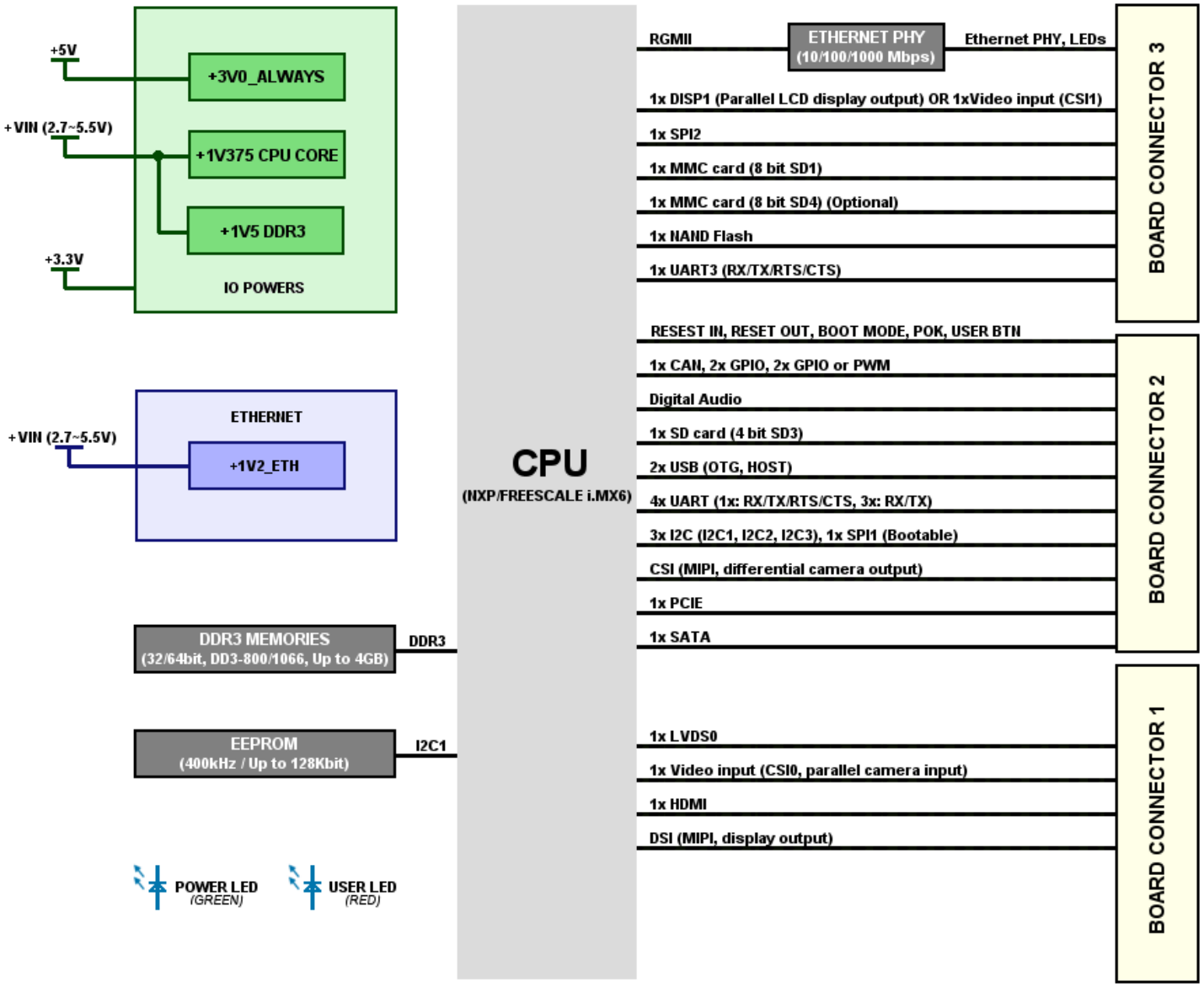
i.MX6 Solo
Single ARM® Cortex®-A9 up to 1.0 GHz
• 512 KB L2 cache, NEON, VFPvd16 TrustZone • 3D graphics with one shader • 2D graphics • 32-bit DDR3 and LPDDR2 at 400 MHz • Gigabit Ethernet MAC • Integrated EPD controller • HDMIv1.4 controller plus PHY • LVDS controller plus PHY • PCIe controller plus PHY • MLB and FlexCAN controllers

i.MX6 Dual
Dual ARM® Cortex®-A9 up to 1.2 GHz
• **1 MB** L2 cache, NEON, VFPvd16 TrustZone • 3D graphics with **four** shaders • **Two** 2D graphics engines • **64-bit** DDR3 and 2-channel 32-bit LPDDR2 at 533 MHz • Gigabit Ethernet MAC • Integrated **SATA-II** • HDMIv1.4 controller plus PHY • LVDS controller plus PHY • PCIe controller plus PHY • MLB and FlexCAN controllers

3. iMX6 TinyRex Signal Description

This chapter describes the signals of the iMX6 TinyRex Module. Some pins have dedicated functionality, but most are highly multiplexed, so that the same pin can have different roles and the same functionality is sometimes available alternatively on different pins. Each of these multiplexed pins is additionally also usable as a General Purpose Input/Output pin (GPIO). Additionally, each GPIO pin can be used as interrupt source.

3.1. iMX6 TinyRex Module Block Diagram



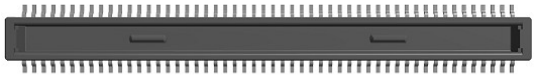
3.2. IO Types Notation

Type	Description	Type	Description
PWR	Power	OD	Open Drain
G	Ground	ODI	ODI - Open Drain Input
I	Input		
O	Output		
I/O	Input / Output		

3.3. J1 - Double Row Pin Header Connector *(CONN HDR 100POS 0.4MM SMD GOLD)*

Description: J1 connector connects the module with the baseboard.
It has space saving design with minimum width and height of the connector.

Manufacturer: Hirose Electric Co. Ltd.
Connector: **DF40C-100DP-0.4V(51)**



Description	Type	PIN Name	PIN	PIN	PIN Name	Type	Description
VIN DC (2.7-5.5V)	PWR	+VIN	1	2	+VIN	PWR	VIN DC (2.7-5.5V)
VIN DC (2.7-5.5V)	PWR	+VIN	3	4	+VIN	PWR	VIN DC (2.7-5.5V)
Ground	G	GND	5	6	+VIN	PWR	VIN DC (2.7-5.5V)
Ground	G	GND	7	8	+VIN	PWR	VIN DC (2.7-5.5V)
Ground	G	GND	9	10	+VIN	PWR	VIN DC (2.7-5.5V)
Ground	G	GND	11	12	+VIN	PWR	VIN DC (2.7-5.5V)
Ground	G	GND	13	14	+VIN	PWR	VIN DC (2.7-5.5V)
Ground	G	GND	15	16	+VIN	PWR	VIN DC (2.7-5.5V)
Ground	G	GND	17	18	+VIN	PWR	VIN DC (2.7-5.5V)
Ground	G	GND	19	20	+VIN	PWR	VIN DC (2.7-5.5V)
Ground	G	GND	21	22	+3V3	PWR	VIN DC (3.3V)
Ground	G	GND	23	24	+3V3	PWR	VIN DC (3.3V)
LVDS Negative Clock Signal	O	LVDS0_CLK_N	25	26	LVDS0_TX0_N	O	LVDS Negative Data Signal
LVDS Positive Clock Signal	O	LVDS0_CLK_P	27	28	LVDS0_TX0_P	O	LVDS Positive Data Signal
Ground	G	GND	29	30	GND	G	Ground
LVDS Negative Data Signal	O	LVDS0_TX2_N	31	32	LVDS0_TX1_N	O	LVDS Negative Data Signal
LVDS Positive Data Signal	O	LVDS0_TX2_P	33	34	LVDS0_TX1_P	O	LVDS Positive Data Signal

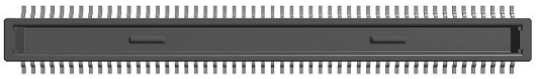
Description	Type	PIN Name	PIN	PIN	PIN Name	Type	Description
Ground	G	GND	35	36	GND	G	Ground
LVDS Negative Data Signal	O	LVDS0_TX3_N	37	38	LVDS0_PWM	IO	GPIO
LVDS Positive Data Signal	O	LVDS0_TX3_P	39	40	LVDS0_CABC	IO	GPIO
Ground	G	GND	41	42	+3V3	PWR	VIN DC (3.3V)
Sensor data latch clock (Pixel Clock)	I	VID_IN_CSI0_PIXCLK	43	44	+3V3	PWR	VIN DC (3.3V)
Sensor data Vertical Sync (Blank Signal)	I	VID_IN_CSI0_VS	45	46	+3V3	PWR	VIN DC (3.3V)
Sensor data Horizontal Sync (Start Of Frame)	I	VID_IN_CSI0_HS	47	48	VID_IN_CSI0_D0	I	Sensor port data
Ground	G	GND	49	50	VID_IN_CSI0_D1	I	Sensor port data
Sensor port data	I	VID_IN_CSI0_D4	51	52	VID_IN_CSI0_D2	I	Sensor port data
Sensor port data	I	VID_IN_CSI0_D5	53	54	VID_IN_CSI0_D3	I	Sensor port data
Sensor port data	I	VID_IN_CSI0_D6	55	56	GND	G	Ground
Sensor port data	I	VID_IN_CSI0_D7	57	58	VID_IN_CSI0_D8	I	Sensor port data
Ground	G	GND	59	60	VID_IN_CSI0_D9	I	Sensor port data
Sensor port data	I	VID_IN_CSI0_D12	61	62	VID_IN_CSI0_D10	I	Sensor port data
Sensor port data	I	VID_IN_CSI0_D13	63	64	VID_IN_CSI0_D11	I	Sensor port data
Sensor port data	I	VID_IN_CSI0_D14	65	66	GND	G	Ground
Sensor port data	I	VID_IN_CSI0_D15	67	68	VID_IN_CSI0_D16	I	Sensor port data
VDC 3V output (Optional Input)	PWR	+3V0_ALWAYS_BB	69	70	VID_IN_CSI0_D17	I	Sensor port data
GPIO	O	VID_IN_CSI0_RSTn	71	72	VID_IN_CSI0_D18	I	Sensor port data
GPIO	I	VID_IN_CSI0_INT	73	74	VID_IN_CSI0_D19	I	Sensor port data
Sensor data Data Enable	I	VID_IN_CSI0_DE	75	76	+5V_BB	PWR	VIN DC (5V)
VOUT DC (3V) (Optional Input)	PWR	+3V0_ALWAYS_BB	77	78	HDMI_HPD	I	HDMI HPD Signal
HDMI Negative Data Signal 1	O	HDMI_D1_N	79	80	HDMI_CEC_IN	O	HDMI CEC line
HDMI Positive Data Signal 1	O	HDMI_D1_P	81	82	HDMI_CEC_STBY	O	GPIO
Ground	G	GND	83	84	+5V_BB	PWR	VIN DC (5V)
HDMI Negative Data Signal 2	O	HDMI_D2_N	85	86	HDMI_D0_N	O	HDMI Negative Data Signal 0
HDMI Positive Data Signal 2	O	HDMI_D2_P	87	88	HDMI_D0_P	O	HDMI Positive Data Signal 0
Ground	G	GND	89	90	GND	G	Ground
DSI differential data line transceiver output 0	I	DSI_D0_N	91	92	HDMI_CLK_N	O	HDMI Negative Clock Signal
DSI differential data line transceiver output 0	I	DSI_D0_P	93	94	HDMI_CLK_P	O	HDMI Positive Clock Signal
Ground	G	GND	95	96	GND	G	Ground

Description	Type	PIN Name	PIN	PIN	PIN Name	Type	Description
DSI differential data line transceiver output 1	I	DSI_D1_N	97	98	DSI_CLK0_N	I	DSI differential clock line transceiver output
DSI differential data line transceiver output 1	I	DSI_D1_P	99	100	DSI_CLK0_P	I	DSI differential clock line transceiver output

3.4. J2 - Double Row Pin Header Connector *(CONN HDR 100POS 0.4MM SMD GOLD)*

Description: J2 connector connects the module with the baseboard.
It has space saving design with minimum width and height of the connector.

Manufacturer: Hirose Electric Co. Ltd.
Connector: **DF40C-100DP-0.4V(51)**



Description	Type	PIN Name	PIN	PIN	PIN Name	Type	Description
Boot mode signal	I	BOOT_MODE1_CON	1	2	RSTINn	I	Reset input
Boot mode signal	I	BOOT_MODE0_CON	3	4	RSTOUTn	O	Reset output
Power good signal Output	O	POK_1V5	5	6	PMIC_ON_REQ	O	Power On request signal
Power good signal Input	I	POK_5V_BB	7	8	ON_OFF	I	ON/OFF signal
Power good signal Open drain Input	ODI	POK_3V3_BB	9	10	USER_BUTTON	IO	GPIO
Ground	G	GND	11	12	GND	G	Ground
GPIO	IO	CPU_GPIO0	13	14	AUD4_CLK	IO	Audio master clock signal
GPIO	IO	CPU_GPIO1	15	16	AUD4_TXC	IO	Audio transmit clock signal
PWM Output Signal	O	GPIO_OR_PWM_1	17	18	AUD4_TXFS	IO	Audio transmit frame sync signal
PWM Output Signal	O	GPIO_OR_PWM_2	19	20	AUD4_TXD	IO	Audio data transmit signal
Ground	G	GND	21	22	AUD4_RXD	IO	Audio data receive signal
SPI clock signal	IO	CSPI1_CLK	23	24	GND	G	Ground
SPI Master data out; slave data in	IO	CSPI1_MOSI	25	26	I2C1_SCL	IO	I2C Serial Clock
SPI Master data in; slave data out	IO	CSPI1_MISO	27	28	I2C1_SDA	IO	I2C Serial Data
SPI Chip select signal	IO	CSPI1_CS0	29	30	FLEXCAN1_TX	O	CAN bus transmit pin
Ground	G	GND	31	32	FLEXCAN1_RX	I	CAN bus receive pin
SD Card detection pin	IO	SD3_CD	33	34	GND	G	Ground
SD Card write protection signal	IO	SD3_WP	35	36	SATA_RX_N	I	SATA Negative receive signal
SD Clock for	O	SD3_CLK	37	38	SATA_RX_P	I	SATA Positive receive signal

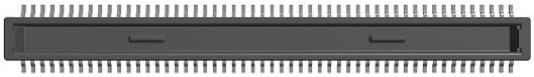
Description	Type	PIN Name	PIN	PIN	PIN Name	Type	Description
MMC/SD/SDIO card							
SD CMD line connect to card	IO	SD3_CMD	39	40	GND	G	Ground
Ground	G	GND	41	42	SATA_TX_N	O	SATA Negative transmit signal
SD Card DATA0 signal	IO	SD3_DATA0	43	44	SATA_TX_P	O	SATA Positive transmit signal
SD Card DATA1 signal	IO	SD3_DATA1	45	46	GND	G	Ground
SD Card DATA2 signal	IO	SD3_DATA2	47	48	I2C2_SCL	IO	I2C Serial Clock
SD Card DATA3 signal	IO	SD3_DATA3	49	50	I2C2_SDA	IO	I2C Serial Data
Ground	G	GND	51	52	I2C3_SDA	IO	I2C Serial Data
UART Serial data transmit	O	UART1_TXD	53	54	I2C3_SCL	IO	I2C Serial Clock
UART Serial data receive	I	UART1_RXD	55	56	GND	G	Ground
UART Request to send	O	UART1_RTS	57	58	UART4_TXD	O	UART Serial data transmit
UART Clear to send	I	UART1_CTS	59	60	UART4_RXD	I	UART Serial data receive
UART Serial data transmit	O	UART2_TXD	61	62	UART5_TXD	O	UART Serial data transmit
UART Serial data receive	I	UART2_RXD	63	64	UART5_RXD	I	UART Serial data receive
Ground	G	GND	65	66	GND	G	Ground
USB OTG Negative transmit signal	IO	USB1_N	67	68	USB0_ID	I	USB OTG ID signal
USB OTG Positive transmit signal	IO	USB1_P	69	70	USB_OC	I	USB overcurrent detection signal
Ground	G	GND	71	72	USB1_PWR_EN	O	USB Power enable signal
USB OTG Negative transmit signal	IO	USB0_N	73	74	USB0_PWR_EN	O	USB Power enable signal
USB OTG Positive transmit signal	IO	USB0_P	75	76	PCIE_WAKE	ODI	GPIO
Ground	G	GND	77	78	GND	G	Ground
PCIE Transmitter Negative transmit signal, Differential pair	O	PCIE_TX_N	79	80	PCIE_CLK_N	O	PCIE Reference Clock Negative transmit Signal, Differential pair
PCIE Transmitter Positive transmit signal, Differential pair	O	PCIE_TX_P	81	82	PCIE_CLK_P	O	PCIE Reference Clock Positive transmit signal, Differential pair
Ground	G	GND	83	84	GND	G	Ground
PCIE Receiver Negative transmit signal, Differential pair	I	PCIE_RX_N	85	86	CSI_CLK0_N	I	MIPI Clock
PCIE Receiver Positive transmit signal, Differential pair	I	PCIE_RX_P	87	88	CSI_CLK_P	I	MIPI Clock
Ground	G	GND	89	90	GND	G	Ground
MIPI Data Lane 2	I	CSI_D2_N	91	92	CSI_D0_N	I	MIPI Data Lane 0
MIPI Data Lane 2	I	CSI_D2_P	93	94	CSI_D0_P	I	MIPI Data Lane 0

Description	Type	PIN Name	PIN	PIN	PIN Name	Type	Description
Ground	G	GND	95	96	GND	G	Ground
MIPI Data Lane 3	I	CSI_D3_N	97	98	CSI_D1_N	I	MIPI Data Lane 1
MIPI Data Lane 3	I	CSI_D3_P	99	100	CSI_D1_P	I	MIPI Data Lane 1

3.5. J3 - Double Row Pin Header Connector *(CONN HDR 100POS 0.4MM SMD GOLD)*

Description: J3 connector connects the module with the baseboard.
It has space saving design with minimum width and height of the connector.

Manufacturer: Hirose Electric Co. Ltd.
Connector: **DF40C-100DP-0.4V(51)**



Description	Type	PIN Name	PIN	PIN	PIN Name	Type	Description
ETH Negative Data Signal 0	IO	TRD0_N	1	2	TRD2_N	IO	ETH Negative Data Signal 2
ETH Positive Data Signal 0	IO	TRD0_P	3	4	TRD2_P	IO	ETH Positive Data Signal 2
Ground	G	GND	5	6	+1V2_BB	PWR	VIN (Optional) Ethernet PHY (1.2V)
ETH Negative Data Signal 1	IO	TRD1_N	7	8	TRD3_N	IO	ETH Negative Data Signal 3
ETH Positive Data Signal 1	IO	TRD1_P	9	10	TRD3_P	IO	ETH Positive Data Signal 3
Ground	G	GND	11	12	+1V2_BB	PWR	VIN (Optional) Ethernet PHY (1.2V)
GPIO	IO	DISP1_INT	13	14	ENET_LED_LINK	O	ETH Link On/Off signal
For async LCD panels	O	DISP1_CS1	15	16	ENET_LED_RX	O	ETH Activity/No activity signal
For async LCD panels	O	DISP1_CS0	17	18	DISP1_RSTn	IO	GPIO
For async LCD panels	O	DISP1_D/CX	19	20	+1V2_BB	PWR	VIN (Optional) Ethernet PHY (1.2V)
For async LCD panels	O	DISP1_RDX	21	22	DISP1_PIXCLK	IO	LCD Pixel clock
For async LCD panels	O	DISP1_WRX	23	24	DISP1_VSYNCH	IO	LCD Frame Sync or Vsync
Ground	G	GND	25	26	DISP1_HSYNCH	IO	LCD Line Pulse or HSync
LCD Data Bus	IO	DISP1_D0	27	28	GND	G	Ground
LCD Data Bus	IO	DISP1_D1	29	30	DISP1_D4	IO	LCD Data Bus
LCD Data Bus	IO	DISP1_D2	31	32	DISP1_D5	IO	LCD Data Bus
LCD Data Bus	IO	DISP1_D3	33	34	DISP1_D6	IO	LCD Data Bus
Ground	G	GND	35	36	DISP1_D7	IO	LCD Data Bus
LCD Data Bus	IO	DISP1_D8	37	38	GND	G	Ground
LCD Data Bus	IO	DISP1_D9	39	40	DISP1_D12	IO	LCD Data Bus
LCD Data Bus	IO	DISP1_D10	41	42	DISP1_D13	IO	LCD Data Bus

Description	Type	PIN Name	PIN	PIN	PIN Name	Type	Description
LCD Data Bus	IO	DISP1_D11	43	44	DISP1_D14	IO	LCD Data Bus
Ground	G	GND	45	46	DISP1_D15	IO	LCD Data Bus
LCD Data Bus	IO	DISP1_D16	47	48	+2V5_BB	PWR	VIN Ethernet PHY DVDDH (2.5V)
LCD Data Bus	IO	DISP1_D17	49	50	SD4_DATA0	IO	SD DATA0 line in all modes Also used to detect busy state
LCD Data Bus	IO	DISP1_D18	51	52	SD4_DATA1	IO	SD Card DATA1 signal
LCD Data Bus	IO	DISP1_D19	53	54	SD4_DATA2	IO	SD Card DATA2 signal
Ground	G	GND	55	56	SD4_DATA3	IO	SD Card DATA3 signal
SD Clock for MMC/SD/SDIO card	O	SD4_CLK	57	58	+2V5_BB	PWR	VIN Ethernet PHY DVDDH (2.5V) (Optional)
SD CMD line connect to card	IO	SD4_CMD	59	60	SD4_DATA4	IO	SD Card DATA4 signal
SD Card write protection pin	IO	SD4_WP	61	62	SD4_DATA5	IO	SD Card DATA5 signal
SD Card detection pin if not used(for the embedded memory),tie low to indicate there is a card attached.	I	SD4_CD	63	64	SD4_DATA6	IO	SD Card DATA6 signal
SD Card write protection pin	IO	SD1_WP	65	66	SD4_DATA7	IO	SD Card DATA7 signal
SD Card detection pin if not used(for the embedded memory),tie low to indicate there is a card attached.	I	SD1_CD	67	68	GND	G	Ground
Ground	G	GND	69	70	CSPI2_CLK	IO	SPI clock signal
UART Serial data transmit	O	UART3_TXD	71	72	CSPI2_MOSI	IO	SPI Master data out; slave data in
UART Serial data receive	I	UART3_RXD	73	74	CSPI2_MISO	IO	SPI Master data in; slave data out
UART Request to send	O	UART3_RTS	75	76	CSPI2_CS0	IO	SPI Chip select signal
UART Clear to send	I	UART3_CTS	77	78	CSPI2_CS1	IO	SPI Chip select signal
Ground	G	GND	79	80	GND	G	Ground
SD Card DATA4 signal	IO	SD1_DATA4	81	82	SD1_DATA0	IO	SD Card DATA0 signal
SD Card DATA5 signal	IO	SD1_DATA5	83	84	SD1_DATA1	IO	SD Card DATA1 signal
SD Card DATA6 signal	IO	SD1_DATA6	85	86	SD1_DATA2	IO	SD Card DATA2 signal
SD Card DATA7 signal	IO	SD1_DATA7	87	88	SD1_DATA3	IO	SD Card DATA3 signal
SD Clock for MMC/SD/SDIO card	O	SD1_CLK	89	90	SD1_CMD	IO	SD CMD line connect to card
Ground	G	GND	91	92	GND	G	Ground
NAND Data signal	IO	NANDF_D4	93	94	NANDF_ALE	O	NAND Address latch enable signal
NAND Data signal	IO	NANDF_D5	95	96	NANDF_CLE	O	NAND Command latch enable signal
NAND Data signal	IO	NANDF_D6	97	98	NANDF_RB0	IO	NAND Ready signal
NAND Data signal	IO	NANDF_D7	99	100	NANDF_WPn	O	NAND Wait polarity signal

3.6. External Connectors

The standard configuration iMX6 TinyRex Module has 3 board-to-board low profile header connectors soldered on the bottom. The recommended 3 mating receptacle connectors (available for purchase at VOIPAC webshop, 3 pcs supplied with each complete development kit) for the custom baseboard interfacing are:

Manufacturer: Hirose Electric Co. Ltd.
Connector: Double Row Receptacle Connector **DF40C-100DS-0.4V(51)**

4. Technical Specifications

4.1. Electrical - Power Consumption

iMX6 TinyRex SOLO module (peak values during booting, the maximum 3W)

iMX6 TinyRex SOLO			
Parameter	**Input Voltage**	**Input Current**	**Input Power**
State	**Vin [V]**	**Iin [A]**	**Pin [W]**
Uboot only	4.99	0.31	1.55
Uboot + ETH	4.97	0.39	1.94
Maximum during booting	4.97	0.6	2.98
Linux idle	4.46	0.33	1.64
Linux + ETH	4.96	0.42	2.08
Stressapptest 1 thread CPU, 1 memory	4.94	0.56	2.77

NOTE: *The tests do not include running HDMI input or GPU. Values may vary depending on the connected peripherals and software version.*

iMX6 TinyRex QUAD module (peak values during booting, the maximum 5W)

iMX6 TinyRex QUAD			
Parameter	**Input Voltage**	**Input Current**	**Input Power**
State	**Vin [V]**	**Iin [A]**	**Pin [W]**
Uboot only	4.96	0.34	1.69
Uboot + ETH	4.95	0.42	2.08
Maximum during booting	4.95	1	4.95
Linux idle	4.43	0.38	1.68
Linux + ETH	4.94	0.46	2.27
Linux + ETH + full HD HDMI – X windows	4.93	0.54	2.66
Stressapptest 4 thread CPU, 4 memory	4.89	0.97	4.74

NOTE: *The tests do not include running HDMI input or GPU. Values may vary depending on the connected peripherals and software version.*

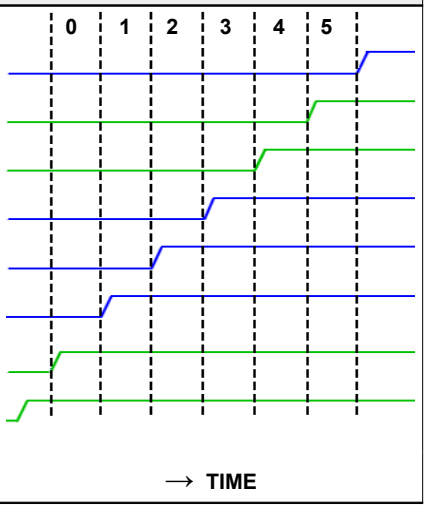
4.2. Electrical - Powering Options

Module powering options		
Simple power	+3V3, +5V	No Ethernet
LIPO battery support	+2.7-5.5V, +3V3, +5V	No Ethernet
Ethernet support	+2.7-5.5V, +3V3, +5V	+2V5, +1V2 Optional

4.3. Electrical – CPU Power Sequencing

CONTROLED BY	NAME	LEVEL	USED BY
POK_3V3_BB (J2-pin9)[*2]	+1V2_ETH[*6*7]	1.2V	Ethernet PHY
POK_2V5_BB[*4]	+3V3[*1]	3.3V	CPU, chips, pull ups
POK_1V5 (J2-pin 5)	+2V5[*5]	2.5V	CPU, Ethernet PHY
POK_1V375	+1V5_DDR	1.5V	CPU, memories
POK_3V0	+1V375	1.375V	CPU, CPU core voltages
POK_5V_BB (J2-pin 7)[*2]	+3V0_ALWAYS[*5*6]	3.0V	CPU, supervisor, pull ups
PMIC_ON_REQ (J2-pin 6)[*3]	+5V_BB[*1]	5V	+3V0_ALWAYS source input, CPU USB
	+VIN[*1]	2.7V-5.5V	Switching power supplies

POWER UP SEQUENCE



Power up sequencing diagram coloring:

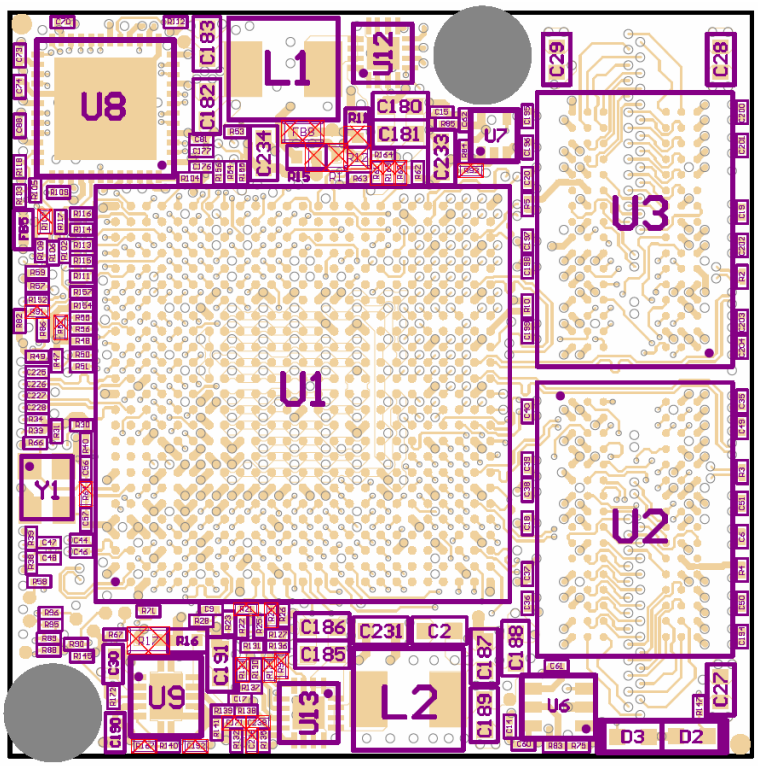
BLUE - power rail or signal generated by module
GREEN - power rail or signal generated by baseboard

(NOTE) ***1 These power rails must be provided by baseboard**
***2 These signals must be provided by baseboard**
*3 Use of this signal is optional
*4 This signal is used internally on baseboard
*5 This power rail can be generated on the module. Testing required
*6 These power rails can be supplied from baseboard
*7 This power rail is not included in the power up sequencing

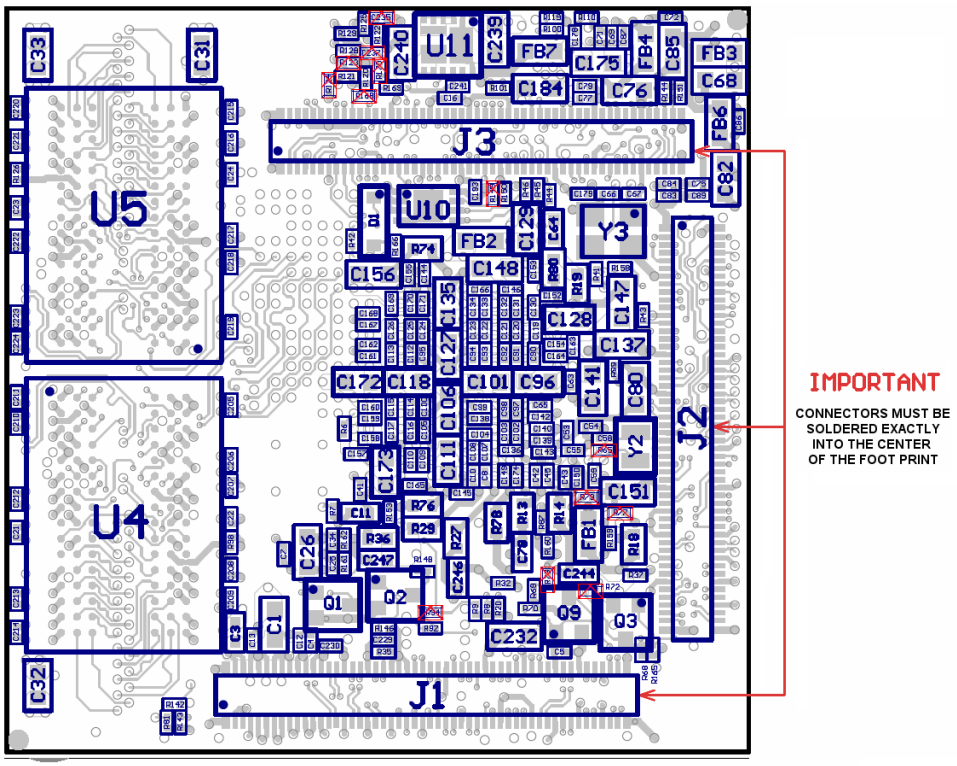
OTHER POWERS	LEVEL	FROM	USED BY
+DDR_VREF	0.75V	+1V5_DDR	ref. for DDR memories, gen. with volt. divider
+1V2_VDD_ARM_CAP	0.950 - 1.250V	CPU	core caps, CPU
+1V1_VDDSOC_CAP	1.175 - 1.250V	CPU	core caps, CPU-sata, CPU-pcie, CPU-hdmi
+VDDPU	1.175 - 1.250V	CPU	core caps

4.4. Mechanical

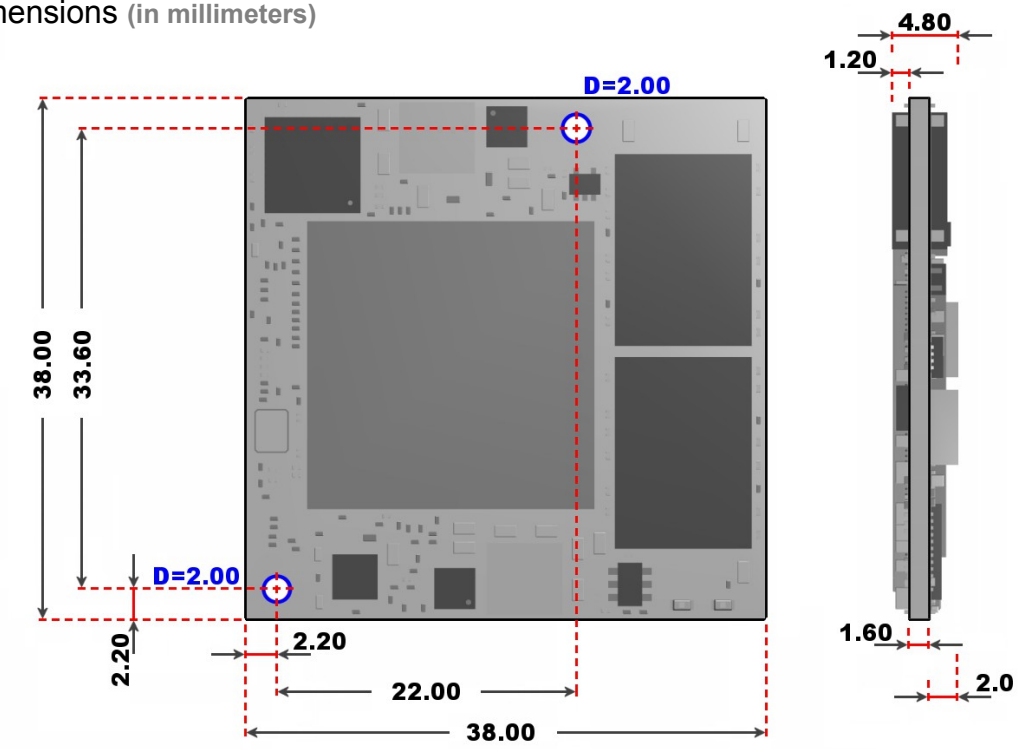
Top Side



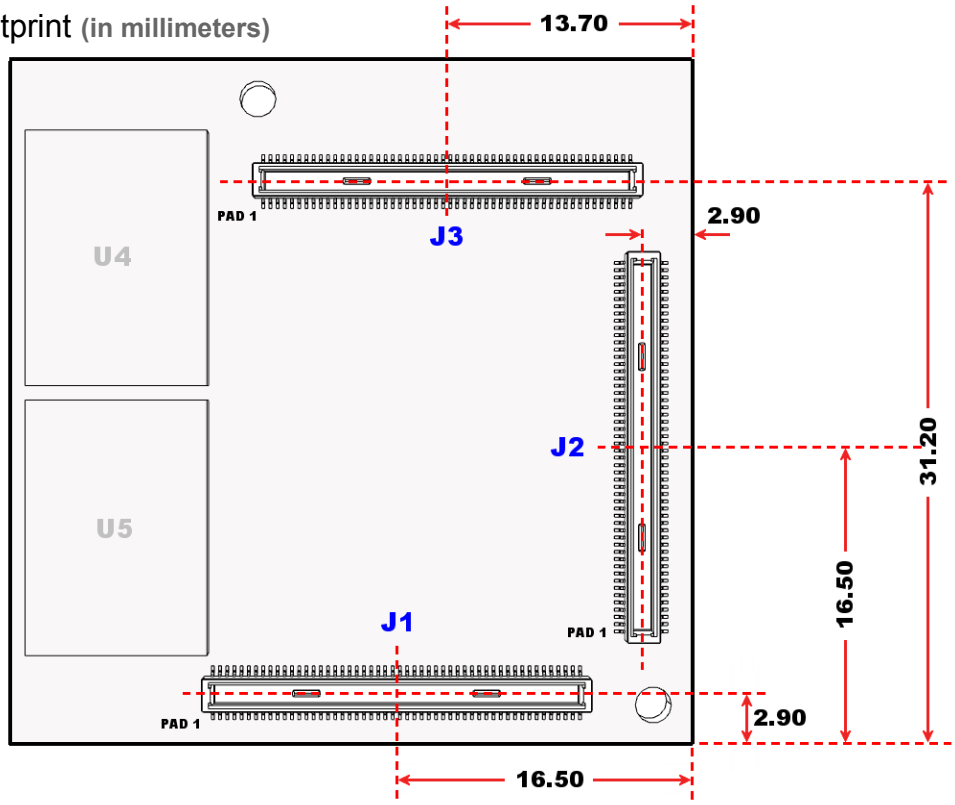
Bottom Side



Dimensions (in millimeters)



Connector Footprint (in millimeters)



4.5. Temperature Range

Symbol	Description	Min	Max	Unit	Standard Unit Range
T_AMB	Operating temperature range - COMMERCIAL	0	+70	°C	X
T_AMB	Operating temperature range - EXTENDED	-20	+70	°C	
T_AMB	Operating temperature range - INDUSTRIAL	-40	+85	°C	

4.6. CE compliance of Voipac products

The CE label is a mandatory conformity mark for complex electronic devices placed on the market in the European Economic Area and each product sold within the EU needs a CE Certificate of Conformance that ensures that the product conforms to the essential requirements of the applicable EC directives.

However, if such complex electronic devices are produced for further processing by the industry, skilled development teams or system integrators, they do not need to observe the above mentioned CE requirements and consequently do not need any identification either. This applies to the Voipac Computers On Module, because these are not used as stand-alone devices by the general public.

To make sure that Voipac COMs can be used in CE marked devices, they are designed to obey the EC directives and the standard configuration SBCs manufactured by Voipac are tested for Electromagnetic Interference and operating temperature ranges plugged in corresponding Base Board and enclosed in a standard Aluminium case provided to Voipac development kits.

4.7. RoHS and WEEE Compliance

All of the products designed and manufactured by VOIPAC TECHNOLOGIES s.r.o. are classified as Electrical and Electronic Equipment (EEE) under the Directive on the restriction of the use of certain hazardous substances in electrical and electronic equipment 2002/95/EC (RoHS). To comply with the RoHS directive, the restricted use of Lead (Pb), Mercury (Hg), Cadmium (Cd), Hexavalent Chromium (Cr 6+), Polybrominated Biphenyls (PBB) and Polybrominated Diphenyl Ethers (PBDE) must be ensured. VOIPAC TECHNOLOGIES s.r.o. guarantees that products ordered after July 1, 2006 are assembled in full compliance with the RoHS directive from the European Parliament and Counsel. The company procedures also complies with the Waste Electrical and Electronic Equipment Directive 2002/96/EC (WEEE) .

Warranty:

VOIPAC TECHNOLOGIES s.r.o. Does Not Bear Responsibility for the Following:

- Failure of a product resulting from misuse, accident, modification, unsuitable operating environment, or improper maintenance by user
- Unless otherwise agreed in written, a product does not include technical support and the customer may be able to purchase technical support under separate agreement
- Any technical or other support provided under warranty by VOIPAC TECHNOLOGIES s.r.o. such as assistance, set-up and installation is provided WITHOUT WARRANTY OF ANY KIND.

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